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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,415	09/20/2000	Kazuyuki Nakagawa	500-0-240	8537

7590 03/17/2004

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Washington, DC 20005-3096

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/665,415	NAKAGAWA ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 01-23-04.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 September 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/23/04 has been entered. An action on the RCE follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US Pat. 6455354) in view of Taguchi et al. (US Pat. 6429372).

Regarding claims 1 and 2, Jiang et al. disclose a semiconductor device comprising:

- a semiconductor element having a primary surface (112 in Fig. 6) with an element electrode (112 and 134 respectively in Fig. 6) and a back surface

- a circuit board/printed circuit board (PCB) having a primary surface (114 in Fig. 6) and a back surface with a board electrode (138 in Fig. 6), the circuit board having a predetermined opening hole (106 in Fig. 6)
- the primary surface of the element being bonded to the primary surface of the circuit board by means of an adhesive layer (108 in an embodiment as shown in Fig. 6), the adhesive layer being of the same size/width as that of the semiconductor element
- the element electrode of the semiconductor element being connected to the board electrode provided on the back surface of the board via the opening hole, and
- the surrounding regions of the side surfaces and back surface of the semiconductor element on the circuit board being sealed with an encapsulate/resin to assume a tapered profile/structure (146 in Fig. 6)

(Fig. 6; Fig. 1-6; Col. 7, line 50- Col. 8, line 60).

Jiang et al. fail to teach the adhesive layer being greater in size than the primary surface of the semiconductor element and the surrounding regions of the side surfaces of the semiconductor element having the sealed resin assuming a flange structure respectively.

Jiang et al. further teach another embodiment (see Fig. 10) where the width/size of the adhesive layer is greater than that of the semiconductor element (see 108 with respect to the die edges 128 in Fig. 10 being extended in width direction; Col. 9, line 10) to provide an improvement in visual inspection and to reduce encapsulation defects (Col. 9, line 5-12; Col. 7-9).

Taguchi et al. teach using an adhesively bonded device having a resin sealing four side surfaces of an integrated circuit (IC) chip (21 and 1 respectively in Fig. 2) and an adhesive layer (6 in Fig. 2) bonding a chip to a tape substrate. Taguchi et al. further teach the adhesive layer being greater in size including length and width dimensions than that of a primary/bonded surface of the IC chip (see 6 in Fig. 2) and being under the resin along four sides/peripheral surfaces of the chip to provide an improved adhesion and bonding (Col. 9, lines 55-63; Col. 10, lines 10-20), the surrounding regions of the side surfaces of the IC chip having the sealed resin being in a flange shape/structure (see shape of 21 in Fig. 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the adhesive layer being greater in size than the primary surface of the semiconductor element the surrounding regions of the side surfaces of the semiconductor element having the sealed resin assuming a flange structure as taught by Taguchi et al. so that the adhesion, stickiness and bonding of the adhesive layer, resin and substrate can be improved in Jiang et al's device.

Regarding claim 3, Jiang et al. and Taguchi et al. teach substantially the entire claimed structure as applied to claim 1, wherein Jiang et al. teach the surrounding regions of the side surfaces and back surface of the semiconductor element being sealed with the resin (146 in Fig. 6).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

03-10-04

NITIN PAREKH

PATENT EXAMINER

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